Claims

We claim:

1. A semiconductor memory test mode configuration, comprising:

a first capacitor for storing digital data connecting a cell plate line to a first bit-line through a first select transistor, the first select transistor activated through a connection to a word line;

at least one reference capacitor for providing a reference voltage to a reference bit-line;

a sense amplifier connected to the first and reference bit-lines for measuring a differential read signal on the first and reference bit-lines; and

a charge path for reducing the differential read signal to determine the signal margin of the semiconductor memory.

2. The semiconductor memory test mode configuration of Claim 1, wherein, after a write of "0" data and read thereof, the first bit-line has a lower signal than the reference bit-line and the charge path increases the charge on the first bit-line.

3. The semiconductor memory test mode configuration of Claim 1, wherein the reference bit-line has a lower signal than the first bit-line and the charge path increases the charge on the reference bit-line.

4. The semiconductor memory test mode configuration of Claim 1, wherein the first bit-line has a higher signal than the reference bit-line and the charge path decreases the charge on the first bit-line.

5. The semiconductor memory test mode configuration of Claim 1, wherein the reference bit-line has a higher signal than the first bit-line and the charge path decreases the charge on the reference bit-line.

6. The semiconductor memory test mode configuration of Claim 1, wherein reference bit-line has a higher signal than the first bit-line and the charge path both decreases the charge on the reference bit-line and increases the charge on the reference bit-line.

7. The semiconductor memory test mode configuration of Claim 1, wherein reference bit-line has a lower signal than the first bit-line and the charge path both increases the charge on the reference bit-line and decreases the charge on the reference bit-line.

8. The semiconductor memory test mode configuration of Claim 1, wherein the charge transfer path includes a third transistor turned on and off to reduce the differential read signal.

8. The semiconductor memory test mode of Claim 1, wherein the first and reference capacitors are ferroelectric capacitors.

9. The semiconductor memory test mode of Claim 1, wherein the first capacitor is part of an FeRAM.

10. A method for testing the signal margin of a semiconductor memory comprising the steps of:

reducing the difference between the amount of charge on a reference bit-line having a voltage supplied by a reference capacitor and on a first bit-line having a voltage provided by an external voltage;

activating a sense amplifier connected to the first and reference bit-lines thereby boosting read signals on the first bit-line representing digital data read from a capacitor and boosting read signals on the reference bit-line; and

determining a reduced differential read signal on the first and reference bit-lines due to the changed amount of charge on the bit-lines.

11. The method of Claim 10 wherein the charges on the reference bit-line and the first bit-line are supplied by ferroelectric capacitors.

12. The method of Claim 10, wherein the capacitor is part of an FeRAM.

13. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises increasing the charge on the first bit-line.

14. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises increasing the charge on the reference bit-line.

15. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises decreasing the charge on the first bit-line.

16. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises decreasing the charge on the reference bit-line.

17. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises both decreasing the charge on the reference bit-line and increasing the charge on the reference bit-line.

18. The method of Claim 10, wherein reducing the difference between the amount of charge on a reference bit-line and on a first bit-line comprises both increasing the charge on the reference bit-line and decreasing the charge on the reference bit-line.